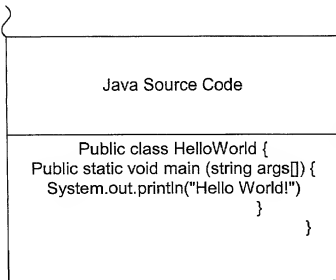
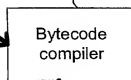


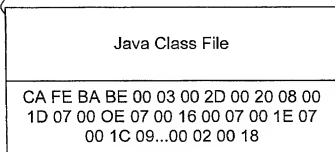
101



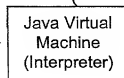
103

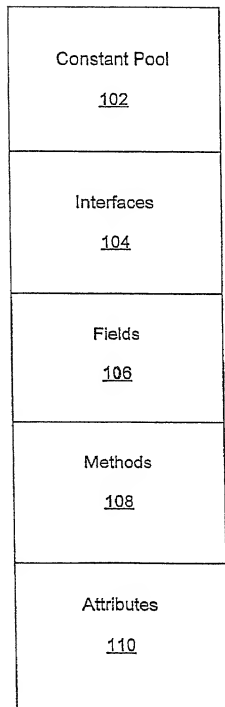


105



107

**Fig. 1A**



100

Fig. 1B

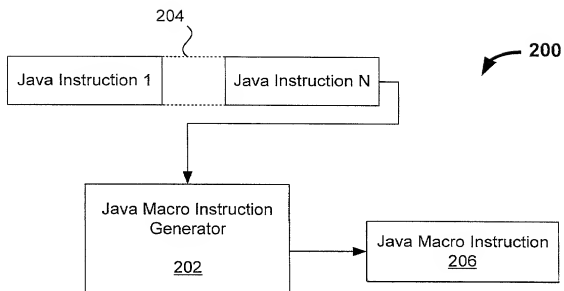


Fig. 2A

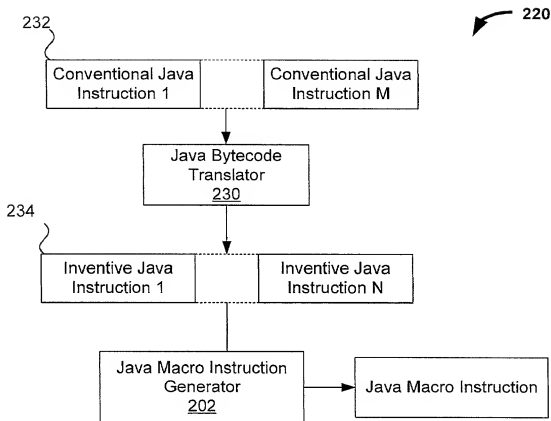


Fig. 2B

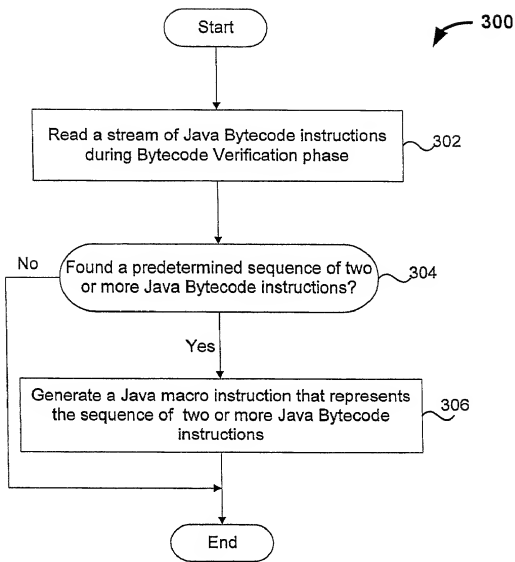


Fig. 3

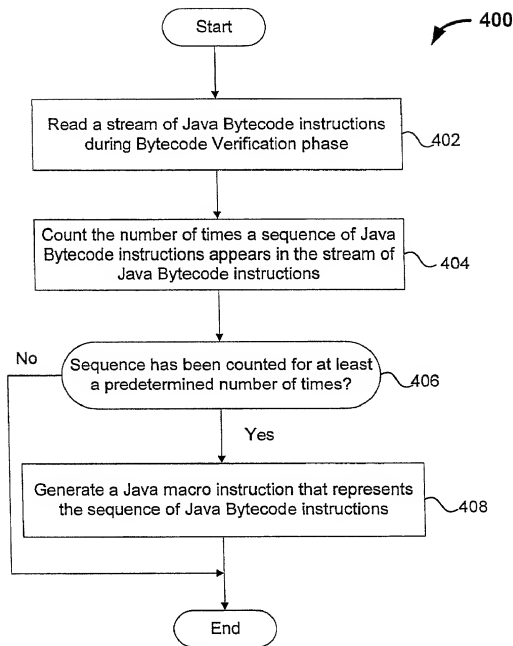


Fig. 4

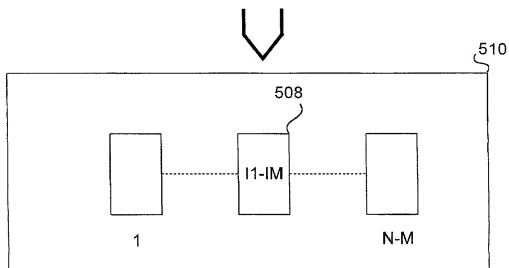
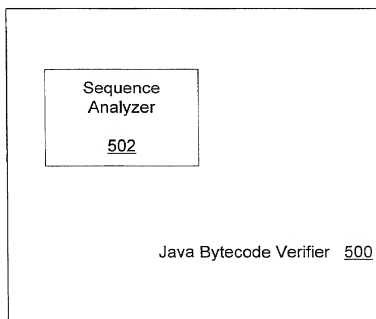
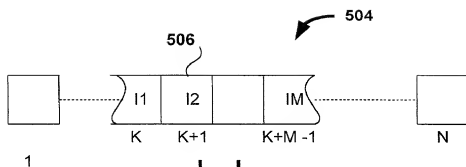


Fig. 5

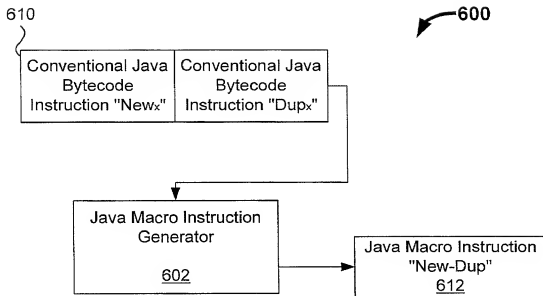


Fig. 6A

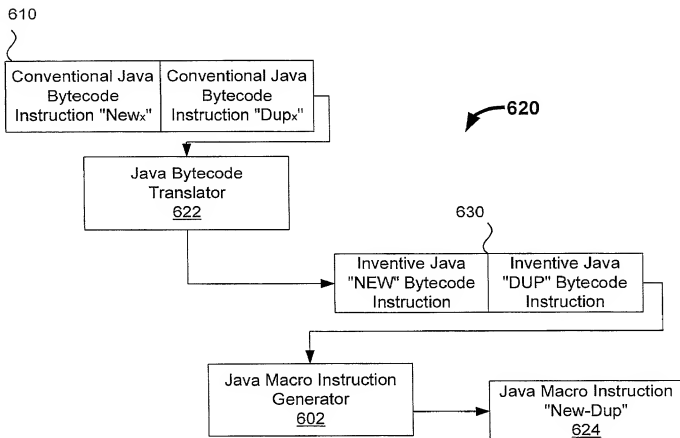


Fig. 6B

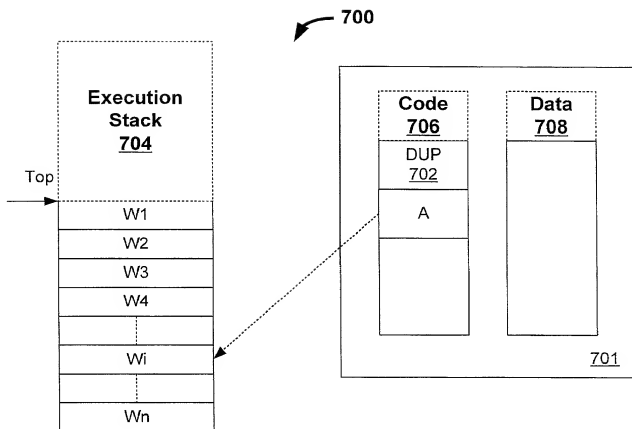


Fig. 7A

DUP

Dup
Dup_x1
Dup_x2

DUPL

Dup2
Dup2_x1
Dup2_x2

NEW

New
Newarray
Anewarray
Multianewarray

Fig. 7B

Fig. 7C

Fig. 8

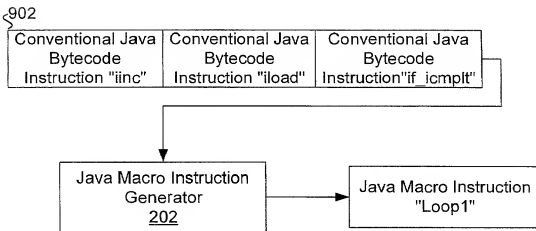


Fig. 9A

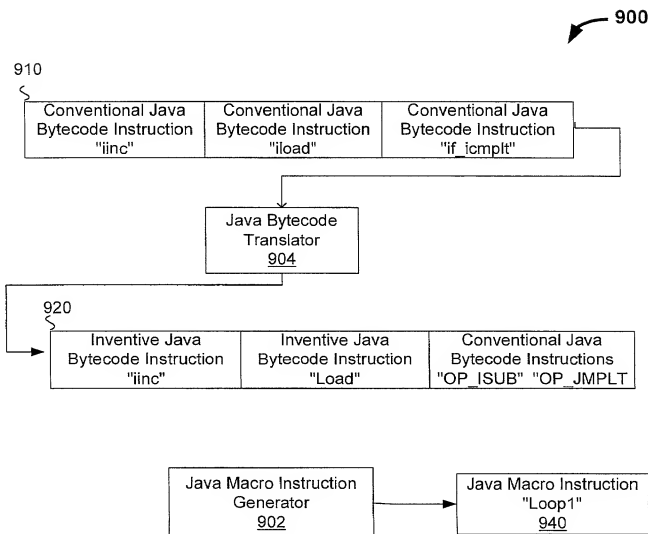


Fig. 9B

The diagram illustrates the memory layout and execution stack. At the top, a memory block is divided into two sections: **Code** (starting at 1002) and **Data** (starting at 1004). The **Data** section contains an **index i** at address 1008. Below this, the **Execution Stack** is shown, starting at address 1020. The stack contains several frames, with the current frame at address 1024 containing **Offset i (A)**. The stack also includes **Offset 0** and **Offset 1**. The stack grows downwards, as indicated by the arrows pointing to the stack frames.

Fig. 10A

LOAD

iload
fload
aload
iload_0
iload_1
iload_2
iload_3
fload_1
fload_2
fload_3
aload_0
aload_1
aload_2
aload_3

LOADL

lload
dload
lload_0
lload_1
lload_2
lload_3
fload_0
dload_0
dload_1
dload_2
dload_3

Fig. 10B

Fig. 10C

lcmp	OP_LSUB, OP_JMPEQ
fcmpl	OP_FSUB, OP_JMPLE
fcmpg	OP_FSUB, OP_JMPGE
dcmpl	OP_DCMP, OP_JMPLE
dcmpg	OP_DCMP, OP_JMPGE

Fig. 11A

if_icmpeq	OP_ISUB, OP_JMPEQ
if_icmpne	OP_ISUB, OP_JMPNE
if_icmplt	OP_ISUB, OP_JMPLT
if_icmpge	OP_ISUB, OP_JMPGE
if_icmpgt	OP_ISUB, OP_JMPGT
if_icmple	OP_ISUB, OP_JMPLE
if_acmpeq	OP_ISUB, OP_JMPEQ
if_acmpne	OP_ISUB, OP_JMPNE

Fig. 11B

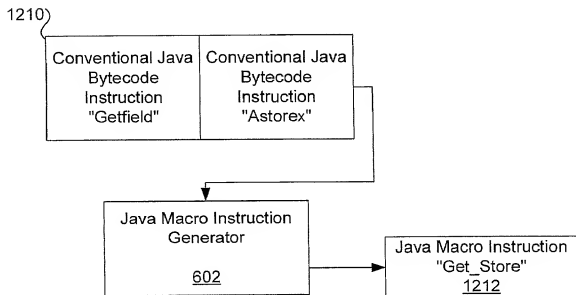


Fig. 12A

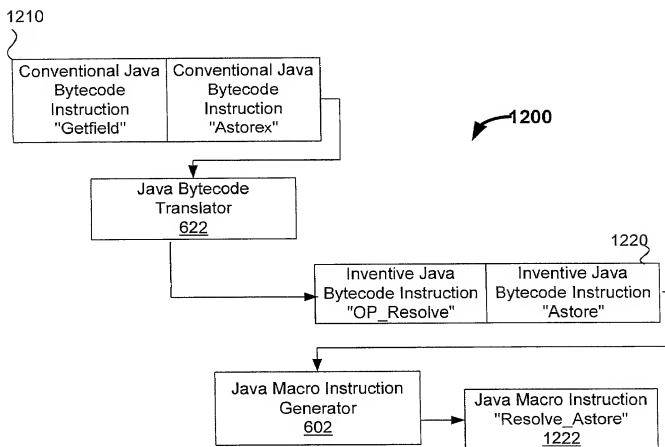


Fig. 12B

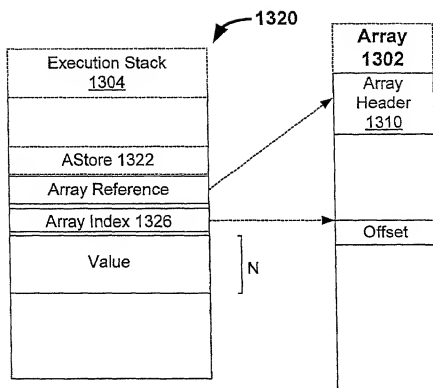


Fig. 13A

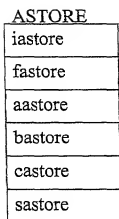


Fig. 13B

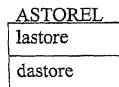


Fig. 13C